We claim:

1. A semiconductor memory device, comprising:

a semiconductor substrate having a first conductivity type and a surface;

an insulating layer disposed on said semiconductor substrate;

a matrix of semiconductor memory elements disposed in said substrate, said semiconductor memory elements including:

a plurality of contact holes formed in said insulating layer, one of said contact holes formed in said insulating layer for each of said semiconductor memory elements;

a bit definition region disposed in said semiconductor substrate underneath each of said contact holes;

a contact plug disposed in each of said contact holes and disposed in electrical contact with said bit definition region, said bit definition region configured such that a contact resistance between said semiconductor substrate and said contact plug defines a bit to be stored in a

respective one of said semiconductor memory elements, said bit definition region in a first group of said semiconductor memory elements is a first implantation region disposed at said surface of said semiconductor substrate and has a dopant of said first conductivity type for decreasing said contact resistance, said bit definition region in a second group of said semiconductor memory elements is a second implantation region disposed at said surface of said semiconductor substrate and has a dopant of a second conductivity type for increasing said contact resistance, and said bit definition region in a third group of said semiconductor memory elements corresponds to said semiconductor substrate;

a further contact region disposed in said semiconductor substrate outside of said bit definition region;

an evaluation circuit connected to and evaluating said contact resistance of said semiconductor memory elements.

2. A method for fabricating a semiconductor memory device, which comprises the steps of:

providing a semiconductor substrate having a first conductivity type;

providing an insulating layer on the semiconductor substrate;

forming a matrix of contact holes down to the semiconductor substrate in the insulating layer in accordance with respective semiconductor memory elements;

providing a surface region of the semiconductor substrate situated underneath each of the contact holes with a contact resistance in accordance with a bit to be stored in a respective semiconductor memory element as a bit definition region of the respective semiconductor memory element, the contact resistance formed by the steps of:

performing a first implantation with a dopant of the first conductivity type into a first group of the contact holes with remaining ones of the contact holes being masked;

performing a second implantation with a dopant of a second conductivity type into a second group of the

contact holes with remaining ones of the contact holes being masked; and

leaving the surface region of the semiconductor substrate situated underneath the respective contact holes in a substrate doping in a third group of contact holes;

providing contact plugs in the contact holes, the contact plugs being in electrical contact with the bit definition region; and

providing a further contact region located in the semiconductor substrate outside the bit definition region.